CLAIMS

1. A dynamically alterable clock comprising:

means for determining if an integer value generated by a microprocessor has a value of 1;

if the integer value is 1, means for sending an input parent clock value to a glitchless clock and sample cycle multiplexer for outputting as an output clock value and means for sending a signal to the glitchless clock and sample cycle multiplexer to output a high signal value as a sample cycle output; and

if the integer value is greater than 1, means for generating a duty-cycle-corrected clock signal from the input parent clock value that has been divided, and sending the duty-cycle-corrected clock signal to the glitchless clock and sample cycle multiplexer for outputting as an output clock value, and means for generating a sample cycle signal, and sending the sample cycle signal to the glitchless clock and sample cycle multiplexer for outputting as a sample cycle value.

2. The clock according to Claim 1 wherein the integer value can be changed dynamically during operation.

3. The clock according to Claim 1 wherein the integer can have a value between 1 and 32.

4. The clock according to Claim 1 wherein the duty-cycle-corrected clock value has a 50% duty cycle.

5. The clock according to Claim 1 wherein the sample cycle output is an enable pulse the width of the input parent clock cycle.

6. A dynamically alterable clock with a rising edge alignment enable signal comprising:

a comparator configured for receiving an integer generated by a microprocessor, determining a value of the integer and sending a bypass signal to a glitchless clock and sample cycle multiplexer if the value of the integer is 1;

a clock divider configured for receiving an input value from an input parent clock when the value of the integer is not 1, dividing the parent clock input, and outputting a clock divider output value;

a duty-cycle corrector configured for receiving the clock divider output value and generating a duty-cycle-corrected clock value;

a sample cycle generator configured for receiving the input parent clock input value when the value of the integer is not 1 and outputting a sample cycle signal; and

a multiplexer comprising:

circuitry configured for receiving as inputs the input parent clock value, the duty-cycle-corrected clock value, the sample cycle signal, and the bypass signal;

circuitry configured for processing the parent clock input when the value of the integer is 1 and outputting an output clock value and a sample cycle output set to a high value; and

circuitry configured for processing the duty-cycle-corrected child clock input when the value of the integer is not 1 and outputting the output clock value and the sample cycle output.

7. The clock according to Claim 6 wherein the integer value can be changed dynamically during operation.

8. The clock according to Claim 6 wherein the integer can have a value between 1 and 32.

9. The clock according to Claim 6 wherein the duty-cycle-corrected clock value has a 50% duty cycle.

10. The clock according to Claim 6 wherein the sample cycle output is an enable pulse having a width of the input parent clock cycle.

11. A glitchless clock and sample cycle multiplexer comprising:

circuitry configured for continuously receiving as inputs an input parent clock value, a duty-cycle-corrected clock value, a sample cycle signal, and a bypass signal;

circuitry configured for processing the input parent clock value when the value of the bypass signal is high and outputting an output clock value based on the input parent clock value and a sample cycle output set to a high value; and

circuitry configured for processing the duty-cycle-corrected clock value and the sample cycle signal when the value of bypass signal is low and outputting an output clock value based on the duty-cycle-corrected clock value and a sample cycle output value based on the sample cycle signal.

12. The multiplexer according to Claim 11 wherein the sample cycle output value is an enable pulse the width of the input parent clock.

13. An glitchless clock and sample cycle multiplexer comprising:

a first NOR gate configured for generating an output clock value, the first NOR gate receiving input from a first AND gate and a second AND gate;

a second NOR gate configured for generating a sample cycle output, the second NOR gate receiving input from a third AND gate a third series of flip-flops;

a first series of flip-flops, comprising at least two flip-flops, each driven by a child clock, and configured for receiving an input from an output of the previous flip-flop in the first series, the first flip-flop in the first series receiving an input from a third NOR

gate coupled to a bypass input and an output from a last flip-flop in a second series of flip-flops, the output of the last flip-flop in the first series inputting to a first AND gate that receives a second input from the child clock;

the second series of flip-flops, comprising at least two flip-flops, each driven by a parent clock, and configured for receiving an input from an output of the previous flip-flop in the second series, the first flip-flop in the second series receiving an input from a fourth NOR gate coupled to an inverted bypass input and the output from the last flip-flop in the first series of flip-flops, the output of the last flip-flop in the second series inputting to a second AND gate that receives a second input from the parent clock; and

at least one flip-flop, driven off the parent clock, and configured for receiving an input from the output of a flip-flop of the second series of flip-flops, the output of the flip-flop inputting to a third NOR gate that receives a second input from the divided sample cycle.

14. A multiplexer for receiving an input parent clock value, a duty-cycle-corrected clock clock, a sample cycle signal, and a bypass signal and outputting an output clock value and a sample cycle value.

15. A method for generating an output clock value and a sample cycle, the method comprising:

receiving an input parent clock value and an integer;

determining if the integer is greater than 1;

if the integer is not greater than 1, sending a bypass signal to a glitchless clock and sample cycle multiplexer and using the input parent clock value as the output clock value and setting the sample cycle to a high state; and

if the integer is greater than 1, dividing and duty-cycle correcting the input parent clock value, sending a duty-cycle-corrected output to the glitchless clock and sample cycle multiplexer for use in generating the output clock value, inputting the integer value

and the input parent clock value to a sample cycle generator, and sending a sample cycle signal to the glitchless clock and sample cycle multiplexer for use in generating the sample cycle output.

16. The method of Claim 15 further comprising dynamically changing the integer value during operation.

17. The method of Claim 15 wherein the integer can have a value between 1 and 32.

18. The method of Claim 15 wherein the duty-cycle-corrected output has a 50% duty cycle.

19. The method of Claim 15 wherein the sample cycle output is an enable pulse the width of the input parent clock cycle.

20. A computer program product for dynamically generating an internal computer clock with a rising edge alignment enable signal, the computer program comprising:

computer program code for calculating an integer value;

computer program code for sending a bypass signal to a glitchless clock and sample cycle multiplexer and using an input parent clock value as an output clock value and setting a sample cycle to a high state if the integer value is 1; and

computer program code for dividing and duty-cycle correcting the input parent clock value, sending a duty-cycle-corrected output to the glitchless clock and sample cycle multiplexer for use in generating the output clock value, generating a sample cycle signal and sending the sample cycle signal to the glitchless clock and sample cycle multiplexer for use in generating the sample cycle if the integer value is greater than 1.